Design of a High Dynamic Range ADC by Concatenating Low Resolution Samples

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Abstract. An innovative method to design a high dynamic range ADC is described. The ADC was developed to acquire audio samples for community noise monitoring with frequencies from 20Hz to 11kHz and a dynamic range which goes from $40dB_{SPL}$ to $140dB_{SPL}$. This ADC module was created to have ADC boards which can be produced nationally with the same performance as imported boards but a lower price. By using low resolution ADCs, some analog amplification and filtering stages, and a concatenation algorithm, a good performance and cost efficient audio sampling module has been built for audio level calculations. In order to guarantee the signal readability a logarithmic legibility formula is introduced. A series of tests with different frequencies and dynamic ranges showed that the module can easily replace the current Sigma-Delta ADC boards.

Keywords: high dynamic range, analog-to-digital converter, concatenation, logarithmic legibility, audio sampling.

1 Introduction

ADCs are always evolving, specially the Sigma-Delta and the Sucesive Approximation architectures. This is mainly because the communications and sensors areas require more precise measurements with greater bandwidths. In the last few years the dynamic range has improved at 1dB per year or 1 equivalent bit every 6 years [1]. Theoric dynamic range can be described as the ratio between the highest amplitude and the smallest amplitude a signal has. Effective dynamic range is the ratio between the highest amplitude and the signal-to-noise level an instrument has.

Noise pollution is a recent problem that affects people, psychologically and physiologically, and noise monitoring is being applied at certain spots in very populated cities in order to know the noise levels and to apply measures to reduce them. The audio signals found in polluted cities have a dynamic range which goes from 20μPa to 200Pa or more, according to what a human can hear. A sound of 200Pa will damage a person's ear almost immediately. The dynamic range of these signals goes from $0dB_{SPL}$ to $140dB_{SPL}$, when calculated with formula (1):

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$$N_p = 10\log_{10}\left(\frac{p^2_{rms}}{p^2_{ref}}\right) = 20\log_{10}\left(\frac{p_{rms}}{p_{ref}}\right), \quad (1)$$

where: N_p is the Sound Pressure Level, p_{rms} is the current pressure level and p_{ref} is the reference pressure level which equals 20μPa.

These audio signals are measured with an IEPE microphone which features high dynamic ranges (140dB$_{SPL}$ or more) and excellent bandwidths (20Hz to 20kHz). The electric signal of the microphone is converted to a discrete signal by using ADC modules. By designing an ADC module with high dynamic range features, further innovations can be applied to obtain a more affordable and full featured board for noise monitoring applications. The theoric dynamic range of an ADC can be calculated with formula (2):

$$\text{ADC Dynamic Range} = 20\log(2^n) + 1.76dB, \quad (2)$$

where: n is the number of bits of binary resolution [3].

According to the dynamic range that sound has, and using formula (2), the number of bits required from an ADC are:

$$140dB = 20\log(2^n) + 1.76dB$$
$$n = \frac{\left(\frac{140dB - 1.76dB}{20}\right)}{\log 2} = 22.96bits \cong 23bits. \quad (3)$$

There certainly are 24 bit ADCs in the market that feature an excellent conversion performance, especially when they work with Sigma-Delta architectures [4]. The main objective of this work was to obtain a new ADC architecture which could be directly compared to existing stronger architectures and could be built by means of common ADCs and analog electronic parts, without the need of complex digital signal processes, such as averaging and approximation, or special signal processing algorithms such as the ones described in [1] and [5].

In order to determine the bandwidth and dynamic range of the ADC, some international standards such as [6] were studied and the features of some other community noise monitors were analyzed [7]. These are the main features that the ADC module had to accomplish (according to IEC 61672 Standard, class 2 of sonometers): a 20Hz to 11kHz bandwidth, a sampling frequency of 22kSps, a dynamic range of 140dB$_{SPL}$, a SNR of 40dB$_{SPL}$, 0.3dB of precision and an analog input voltage up to 10V$_{rms}$.

2 Concatenated ADC Architecture

The Concatenated ADC amplification stages are depicted in Fig. 1. The signal is amplified 16 times per stage. A low offset operational amplifier (OP177GP with V_{OS}<60μV) was used in order to avoid the offset from being amplified stage by stage

and to prevent clipping at further stages. The fifth stage will always have a high offset, so an anti-offset filter was added to attenuate this DC value.

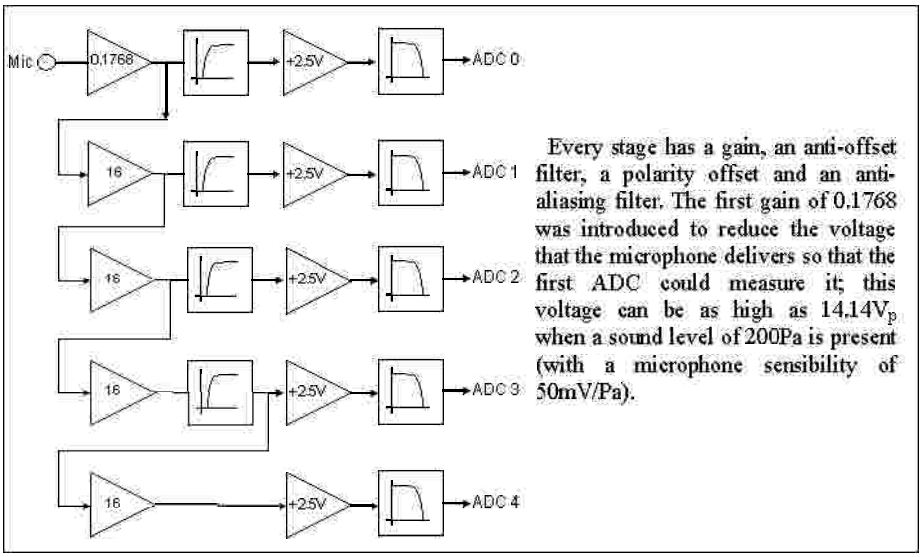


Fig. 1. Concatenated ADC amplification stages.

It is important that the signal, which is amplified in every stage, keeps a low delay between stages. If an anti-offset filter was added to the last stage, then the same filter should be added to every previous stage to keep a constant delay between them. These anti-offset filters are high-pass with a 1-order curve and a -3dB point at 20Hz.

After the signal has been amplified, a positive offset of 2.5V must be added to it so that the unipolar ADCs can measure it within a range from 0V to 5V. An anti-aliasing group of filters with a cutoff frequency at 11kHz are added just before every ADC.

If the instantaneous signal is so low to be measured by the low resolution ADC in the first stage, then the next measurement will be tested, now that the voltage is greater than the one in the first stage. If the second ADC can't measure it, then the third ADC should give it a try. And so on, until the fifth stage should be able to measure it.

In order to define when a voltage is measurable by an ADC or not, lineal and logarithmic legibility should be calculated. Lineal legibility is the smallest measurement that an ADC can present. It can be calculated by using formula (4).

$$\mathrm{Leg}_{\mathrm{L}} = \frac{V_{\max\, scale}}{2^{n} - 1}, \tag{4}$$

where: $V_{max\ scale}$ is the highest value that the ADC can measure and n is the number of bits that the ADC has.

As a first approach, a 9 bit theoric ADC is chosen to determine if it can present good legibilities. Its lineal legibility (also known as sensibility) is calculated with formula (4):

$$\text{Leg}_{\text{L}} = \frac{2.5V}{2^9 - 1} = 4.89mV / bit, \tag{5}$$

Logarithmic legibility is the smallest measurement in dB units that an ADC can present and it is calculated by using formula (6).

$$\text{Leg}_{\text{dB}} = 20\log(V_{\min scale} + Leg_L) - 20\log V_{\min scale} =$$

$$\text{Leg}_{\text{dB}} = 20\log\left(\frac{V_{\min scale} + Leg_L}{V_{\min scale}}\right), \tag{6}$$

where: $V_{\min \text{ scale}}$ is the smallest value to measure on the ADC lineal scale.

If $V_{\max \text{ scale}}$ is 2.5V and a $V_{\min \text{ scale}}$ value of (1/16)($V_{\max \text{ scale}}$) is chosen, then the logarithmic legibility is as follows:

$$\text{Leg}_{\text{dB}} = 20\log\left(\frac{156.25mV + \frac{2.5V}{511}}{156.25mV}\right) = 0.2677dB, \tag{7}$$

where 0.2677dB are smaller than the ±0.3dB proposed for the logarithmic precision of the ADC module. It is well known that most ADCs have noise in their 2 LSB (differential and nonlinearity issues) and the logarithmic legibility can get worsened by that. By adding 2 bits of resolution to the ADC this problem can be avoided and the Leg_{dB} can be improved:

$$\text{Leg}_{\text{dB}} = 20\log\left(\frac{156.25mV + \frac{2.5V}{2047}}{156.25mV}\right) = 0.0676dB. \tag{8}$$

A resolution of 11 bits should be enough to guarantee a $0.3\text{dB}_{\text{SPL}}$ precision on a single polarity signal, but the microphone delivers positive and negative signals. To add negative polarity support, an extra 1 MSB should be added to the ADC, requiring then 12 bits of resolution. The ADCs chosen for this project were the MCP3201 produced by Microchip. The MCP3201 features an SAR architecture with 12 bits of resolution and 100kSps of sampling frequency.

Now that Leg_{dB} is guaranteed, Leg_{L} must be improved. Previous calculations showed that a 9 bit ADC has a 4.89mV/bit legibility which is not enough to measure the 100µV of a 40dB_{SPL} signal (with a microphone sensibility of 50mV/Pa and 2mPa of sound pressure). In order to improve the Leg_{L} the amplification stages are used.

If an instantaneous voltage level in the first amplification stage is greater than 1/16, then that level will be legible and the ADC can measure it with good Leg_{dB}, but if the voltage is lower than 1/16, then the next ADC will have to measure it. Every stage has the same legibility set point at 1/16 as shown in Fig. 2. When the signal is taken from the last stage, it is because its magnitude was lower than 3.05mPa. A level of 40dB_{SPL} or 2mPa is lower than the maximum scale at the last stage, therefore, a theoric dynamic range of 40dB_{SPL} is guaranteed.

A simultaneous measurement has to be taken from every stage by every ADC. By having 5 simultaneous samples a legible sample can be chosen, so that the instantaneous signal doesn't change while the microcontroller is choosing an ADC channel.

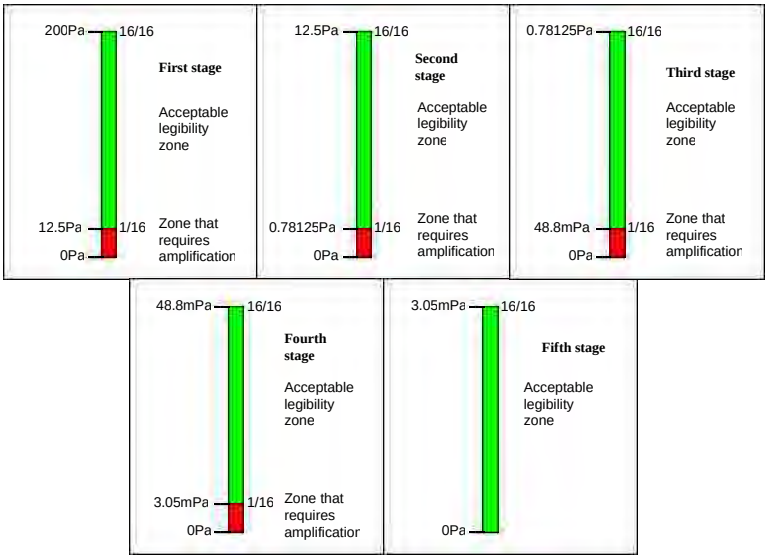


Fig. 2. Amplification stages used in a Concatenated ADC.

Choosing a legible sample from all 5 channels is easily done. Considering that every ADC has 2048 steps due to its binary resolution on one polarity, the non legible zone is delimited by 1/16 of 2048. The ADC originally has 4096 steps, where the first 2048 contain the negative polarity signal, and the last 2048 ones contain the positive one (see Fig. 3).

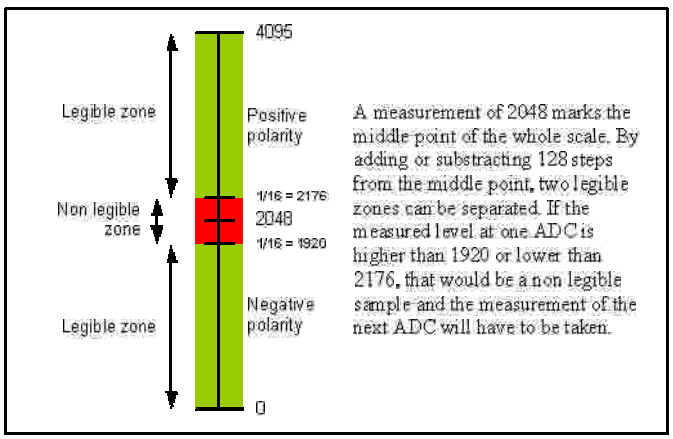
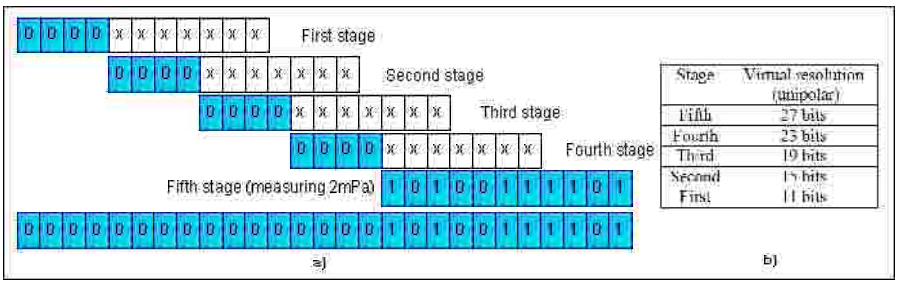


Fig. 3. Legible zones in both polarities.

Once that a legible sample has been found it can be concatenated into a higher resolution sample by adding zeroes depending on which stage it was located and taking advantage of the 2^4 gain. For instance, if a sample had a level of 2mPa it would be located in the fifth stage as seen in Fig. 4 (a). The microcontroller will take the measurement of the first stage and will determine if that level is lower than 1/16 of the $V_{max\ scale}$. It is known that every bit in a binary sample equals one half of a scale. If the MSB is 1, the sample is located at the upper half, and if it's 0 it's located in the lower half. The current measurement is lower than 1/16, and then the MSB will be 0. The next bit represents a fourth of the scale, it will be a zero since the sample is still lower than 1/4. The next two bits, the eighth and sixteenth portions will also be zeroes. Now it is known that the first ADC does not have enough Leg_{dB} to measure the sample.



Stage	Virtual resolution (unipolar)
Fifth	27 bits
Fourth	23 bits
Third	19 bits
Second	15 bits
First	11 bits

Fig. 4. Concatenation of a legible sample into non legible samples.

From stage 1 to stage 4, there will be 4 zeroes from every ADC and the last stage will have 11 legible bits. According to these facts, a virtual improved resolution is obtained depending on which stage contains the legible sample. The stage resolution is showed in Fig. 4 (b). An extra MSB must be added to indicate the signal polarity; therefore, a maximum of 28 bit virtual resolution can be obtained if a signal is located at the fifth stage. The virtual lineal legibility is calculated as follows:

$$\mathrm{Leg_L} = \frac{(10V_{rms})(\sqrt{2})}{2^{27}-1} = 105.36nV/bit, \tag{9}$$

which is lower than the 100μV that a $40dB_{SPL}$ signal has.

The 12 bit resolution and the minimum scale voltage of 1/16 are a good combination since 12 bit ADCs and an array of 5 amplification stages are easy to implement. The greater the number of amplification stages implemented, the lower ADC resolution is required. The greater the ADC resolution used, the smaller the logarithmic legibility.

3 ADC Module Performance

Once that the ADC module was assembled, a series of dynamic range and bandwidth tests were performed with a signal generator. An application was programmed with Visual C# 2008 in order to connect the board via USB, stream the legible samples,

calculate the equivalent continuous sound level and plot the signals in time and frequency domains. The frequency domain plot was calculated with regular windows such as Hamming and Hanning, or the Nuttall high dynamic range window [8].

Table 1 shows the frequency response of the module when tested with a 114dB$_{SPL}$ signal. The -3dB frequency begins at 20Hz due to the anti-offset filter and the second -3dB point is found at 11kHz according to the anti-aliasing filter (see Fig. 5). A 20Hz to 11kHz bandwidth was achieved with an acceptable precision.

Table 1. ADC module frequency response.

Frequency (Hz)	dB$_{SPL}$	Gain (dB)	Frequency (Hz)	dB$_{SPL}$	Gain (dB)
10	107.17	-6.83	800	113.99	-0.01
20	111	-3	1000	113.99	-0.01
30	112.39	-1.61	1250	113.97	-0.03
50	113.32	-0.68	1600	113.93	-0.07
80	113.73	-0.27	2000	113.91	-0.09
100	113.84	-0.16	2500	113.82	-0.18
150	113.95	-0.05	3150	113.71	-0.29
160	113.96	-0.04	4000	113.5	-0.5
200	113.98	-0.02	5000	113.29	-0.71
250	113.99	-0.01	6300	112.97	-1.03
315	114	0	8000	112.39	-1.61
400	114	0	10000	111.5	-2.5
500	113.99	-0.01	10900	111.07	-2.93
630	114	0			

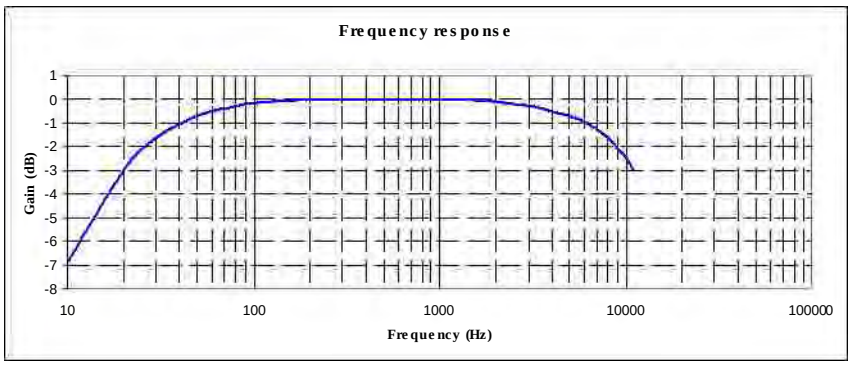


Fig. 5. Frequency response of the concatenated ADC module.

The signal-to-noise level of the module was tested with a 0V signal. An image of this signal is shown in Fig. 6. A level of 35dB$_{SPL}$ was found, which is better than the 40dB$_{SPL}$ proposed.

Further levels were tested with a constant frequency signal of 1kHz and a dynamic range from 49dB$_{SPL}$ to 135dB$_{SPL}$ (see Fig. 7 and 8). Distortion levels were found in the range from 49dB$_{SPL}$ to 69dB$_{SPL}$ due to the very small amplitude that the signal generator had to output, but the signals were correctly measured and plotted.

Some phase delays were observed between stages, when a stage was switched to a higher or lower one. These delays were given by the difference between the RC values on each anti-offset filter and by the opamp delay. Although the phase delay of the original signal is affected by the anti-offset and anti-aliasing filters, there are no definitive studies that demonstrate that phase delays significantly affect the quality of the signal when heard by a human [9], so the digital signal can still be used to measure noise levels.

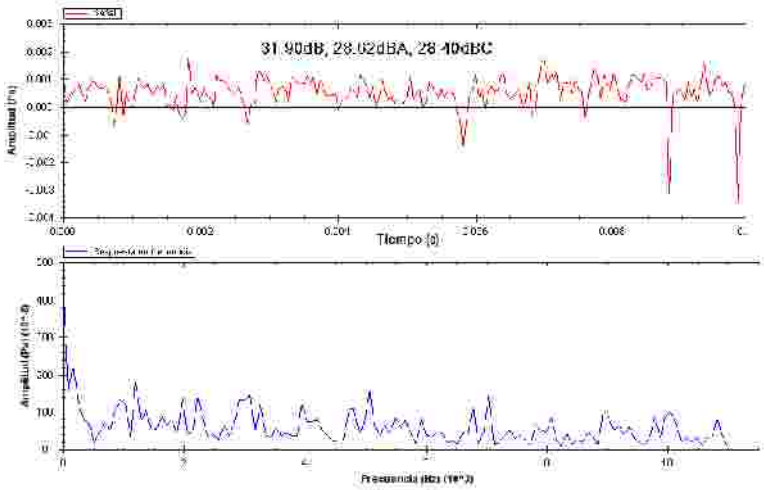


Fig. 6. Signal-to-noise level of the ADC Module.

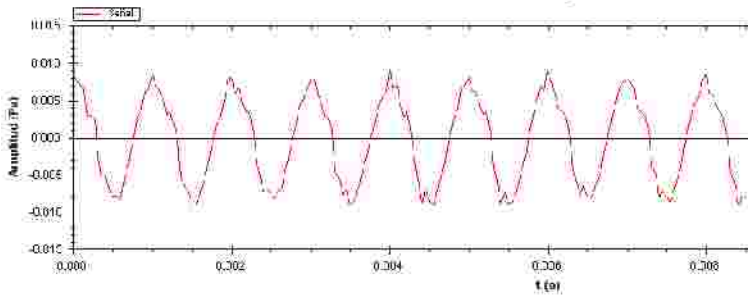


Fig. 7. A 49dB$_{SPL}$ (500μV @ 1kHz) signal measured by the ADC module.

A theoric dynamic range of 167dB was calculated by using formula (2):

$$\text{Dynamic Range} = 20\log\left(2^{27}\right) + 1.76dB = 164.3dB. \quad (\mathbf{10})$$

An effective dynamic range of 105dB was obtained by substracting 35dB (SNR) from 140dB. The bandwidth (20Hz to 11kHz) and dynamic range ($40dB_{SPL}$ to $140dB_{SPL}$) were accomplished with low resolution ADCs and simple analog filtering and amplification stages.

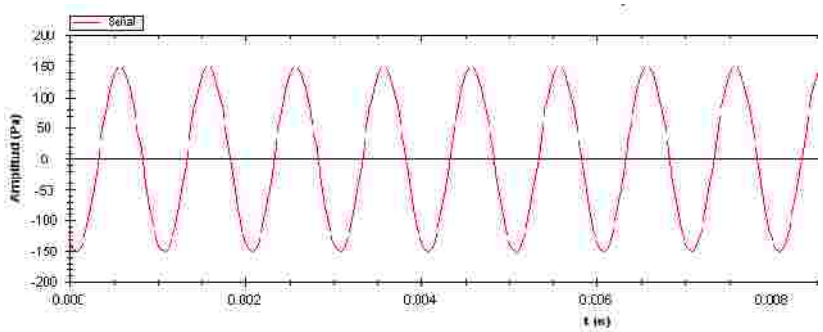


Fig. 8. A $135dB_{SPL}$ (6.84V @ 1kHz) signal measured by the ADC module.

4 Discussion

The applied tests on the ADC module showed that it can measure audio levels from 20Hz to 11kHz with very good precision. This ADC module can be compared to other commercial modules with similar features. Table 2 shows these features.

The National Instruments NI USB 9233 is an over-featured board when used for noise monitoring, since audio sampling requires up to 32kSps (according to [6]) and only one input channel. A sampling frequency of 22kSps is enough since some noise monitoring experiments that have been done, showed that signals with significant amplitudes are only present at up to 8kHz.

The theoric dynamic range of the Concatenated ADC is better than the NI USB since it has more resolution bits, but the effective dynamic range is almost similar to the NI USB. Both ranges can compress an audio signal ranging from $40dB_{SPL}$ to $140dB_{SPL}$.

Table 2. Concatenated ADC module vs. NI USB 9233.

	NI USB 9233	ADC Module Prototype
Sampled channels	4	1
Sampling frequency	up to 50kSps	22kSps
Resolution	24 bits	27 bits plus sign
Theoric dynamic range	146dB	164dB
Effective dynamic range	98dB (25kSps)	105dB (22kSps)
ADC architecture	Delta-Sigma	Concatenated ADC
AC Cutoff Frequency	0.5Hz	20Hz
Input Voltage Range	$\pm 5.8V_p$	$\pm 14.14V_p$
Precision	0.6dB (no calibration)	$\pm 0.2677dB$, according to Leg_{dB}

The sampling frequency of the prototype was limited due to the PIC microcontroller used, which has a 12MIPS speed. If a faster microcontroller or a digital signal processor was used, then a 32kSps speed could be achieved and a Class 1 Sonometer could be integrated within the module.

5 Conclusions

The concatenated ADC that has been proposed and designed in this work can be used on signals that have bandwidths a little beyond the 0Hz frequency due to the anti-offset filtering required. No DC measurements can be done with this ADC architecture. The minimum scale voltage and the number of ADC resolution bits mark the balance between amplification stages and logarithmic legibility.

A phase delay between stages can be made almost zero if the RC values are similar between stages. This is achievable by implementing low tolerance elements with 1% of precision or less.

A virtual resolution of 27 bits plus sign was obtained by concatenating the measurements of each stage. Simultaneous ADC samplings are required in order to prevent samples loss and effective concatenations.

These concatenations imply the adding of zeroes to the left or right of the legible sample if the minimum scale voltage is a power of 2 (for example, 1/16 or 1/32). A microcontroller can easily add these zeroes by shifting the value to the left or right. When a sample is found legible in the first stage, zeroes are added to the right. When it is found on the second, third or fourth stages, zeroes are added on both sides. When it is found on the last stage, zeroes are added to the left.

Logarithmic legibility indicates whether a signal can be correctly measured in a logarithmic scale and achieve a good precision, depending on the application requirements.

A bessel analog filter can be implemented instead of the 1-order anti-offset filter used. This filter would have a phase delay present beyond the bandwidth of the signal to be measured. The phase delay between stages would almost disappear.

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